REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on September 12, 2003, and the references cited therewith.

No claims are amended, canceled, or added; as a result, claims 1-12, 14-19, and 21-23 are now pending in this application.

37 C.F.R. §1.83(a) Objection to the Drawings

The drawings were objected to because of the claimed feature of a hardware based pulse width modulator. This objection is respectfully traversed. The application clearly describes and shows hardware in FIG. 10 in block form. Page 10, lines 26 et seq. clearly describe a hardware implementation: "Fig. 10 contains a block diagram of an LED backlight 901 and associated drive electronics. LED backlight 901 is coupled to the positive and negative poles 904a and 904b of a power supply. In a preferred embodiment of the invention, a driver 912 and buffer 910 switch on and off in response to a control pulses 908 output by a pulse width modulator 916." In this context, one embodiment is clearly described as electronics, which is also known as hardware to those of skill in the art. Thus, this rejection should be withdrawn, and no new drawings required.

Objection to the Specification

The disclosure was objected to on page 4, lines 9-11 because the definition of PWM duty cycle contradicts Equation (1) on page 6. The language on page 4 has been amended to be consistent with Equation (1). As such, no new matter is introduced. Similarly, language on pages 9 and 10 have been amended to overcome the objections without the introduction of new matter.

§112 Rejection of the Claims

Claims 21-23 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This rejection is respectfully traversed. As indicated above with respect to the

discussion of the drawing, a hardware based pulse width modulator is clearly described with respect to Fig. 10. Further, on page 5, a specific reference to hardware is included: "Absent the present invention, the only way to achieve the desired resolution is to change the pulse width modulator to one having three bit or higher resolution. Changing the **hardware** in such fashion may be impractical because the desired hardware is unavailable or costly due to the associated hardware and software changes." Emphasis added. Since this was the only rejection of these claims, it is respectfully requested that they be allowed.

§103 Rejection of the Claims

Claims 1-2, 4-6, 8-9, 11-12, 14-17, 19 were rejected under 35 USC § 103(a) as being unpatentable over Zuraski et al. (U.S. Patent No. 5,589,805) in view of Akiko (JP 04-096417). This rejection is respectfully traversed on the basis that Zuraski et al. and Akiko either alone or combined do not show, teach or suggest each and every element of the invention as claimed.

Zuraski et al. indicates that "a predetermined control period (T_c) provides regular intervals of adjustment for the PWM_n output state in accordance with a set of program instructions not germane to the present invention nor necessitating further discussion herein", at Col. 5, lines 9-12. Thus, Zuraski et al. clearly lacks the last element of claim 1: "establishing a pulse width modulation update interval of $K*P_T$." The update interval is clearly a function of the number of additional states. Zuraski et al., only "varies between adjacent discrete PWM_n output states, (s) and (s + 1) within such control period T_c" Col. 5, lines 19-21. The presently claimed invention in claim 1 recites "associating a modulator output value with each one of the said K states", which allows multiple different states during a time period that is a function of the additional states.

The Examiner agrees that Zuraski et al. does not show an additional timer to generate K associated states, wherein K is greater than 2 and establishing a pulse width modulation update interval $K*P_T$. It is then stated that "Akiko teaches a timer with an 8-bit resolution is used and PWM output having a resolution of 10-bits (See Figs. 2, 5, items 1-2 in Detailed Description See Page 1, last paragraph and Page 3, 1st paragraph)." It is not clear why additional timer resolution and a 10-bit PWM output resolution teach or show these missing elements. Akiko, in the

translation provided, states that when the timer register value is equal to a value in a comparison register at the bottom of page 1, a timer interrupt is generated and PWM output is carried out. This language does not describe the pulse width modulation update interval that is claimed, and thus does not allow multiple different states during a time period. Page 3 of Akiko indicates that the table of Figure 2 contains the average values of the values set in the comparison register. Average values do not teach or suggest establishing a pulse width modulation update interval $K*P_T$ as claimed. Thus, since the combination of the references do not teach or suggest each and every element of claim 1, the rejection should be withdrawn.

Claims 2-4 depend from claim 1 and are believed allowable at least for the same reasons. Further reference cited with respect to some of these claims do not provide the missing elements.

Claim 5 recites "outputting a pulse according to said modulator output value during each time period P_n occurring within said timer period P_T during each one of said K timer states". This is clearly not provided by Zuraski et al., nor Akiko as previously described. Claims 6-10 depend from claim 5 and are believed allowable for at least the same reasons.

Claim 11, along with dependent claim 12 also contain a recitation about assigning a modulator output value with each one of said K states, wherein K is greater than 2. Since the claims are written in a means plus function format, they are interpreted to include the structure that accomplishes the function described in the application and equivalents thereof. This structure corresponds to the structure in FIG. 10, and its functions described with respect to the remaining Figures. In particular, it includes the multiple additional states used within a period P_T, which is a multiple of the PWM period. None of the references teach or suggest this, and the rejection should be withdrawn.

Claim 14 also recites K greater than 2, and the outputting of a plurality of pulses according to modulator output values to obtain a resolution dependent on K. Thus, it clearly distinguishes over the references, since Zuraski et al. only utilizes adjacent output states during a period, and Akiko also lacks such teaching. Claims 15-18 depend from claim 14, and are believed allowable for at least the same reasons.

Claim 19 is similar to claim 14 and is allowable for at least the same reasons.

Claims 3, 7, 10, 18 were rejected under 35 USC § 103(a) as being unpatentable over Zuraski et al. and Akiko as aforementioned in claims 1, 5, 14 in view of Shibuya et al. (U.S. Patent No. 6,191,868). These claims are believed allowable as indicated above since they depend from claims that are believed allowable, and Shibuya et al. does not provide the element or elements missing from Zuraski et al. and Akiko.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6972 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 14 day of October, 2003

Gina M. Uphus _____

Name Signature